



正基科技股份有限公司

SPECIFICATION

PRODUCT NAME : AP5256

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Customer APPROVED	
Company	
Representative Signature	

PREPARED	REVIEW			APPROVED	DCC ISSUE
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正基科技股份有限公司



AP5256 Data Sheet

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Revision

Revision	Date	Description	Revised By
1.0	2018 / 10 / 05	- Preliminary	Harry
1.0.1	2019 / 05 / 22	- Modify BT Spec.	Richard
1.1	2019 / 06 / 17	- Modify Module Dimensions	Eason
1.2	2019 / 07 / 30	- Add Module bottom view in Dimensions	Richard
1.3	2019 / 11 / 18	- Modify Package Information	Richard
1.4	2019 / 12 / 09	- Modify Pin Assignment - Modify External clock reference	Richard
1.5	2020 / 03 / 02	- Modify 5GHz RF Specification	Ali
1.6	2020 / 07 / 27	- Modify Module Dimension	Eason
1.7	2021 / 03 / 29	- Amend company address	Eason
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2.1	2024/ 06 /26	- Modify 37.4MHz X'TAL characteristics	Ali
2.2	2024/ 06 /27	- Modify 37.4MHz X'TAL characteristics	Ali



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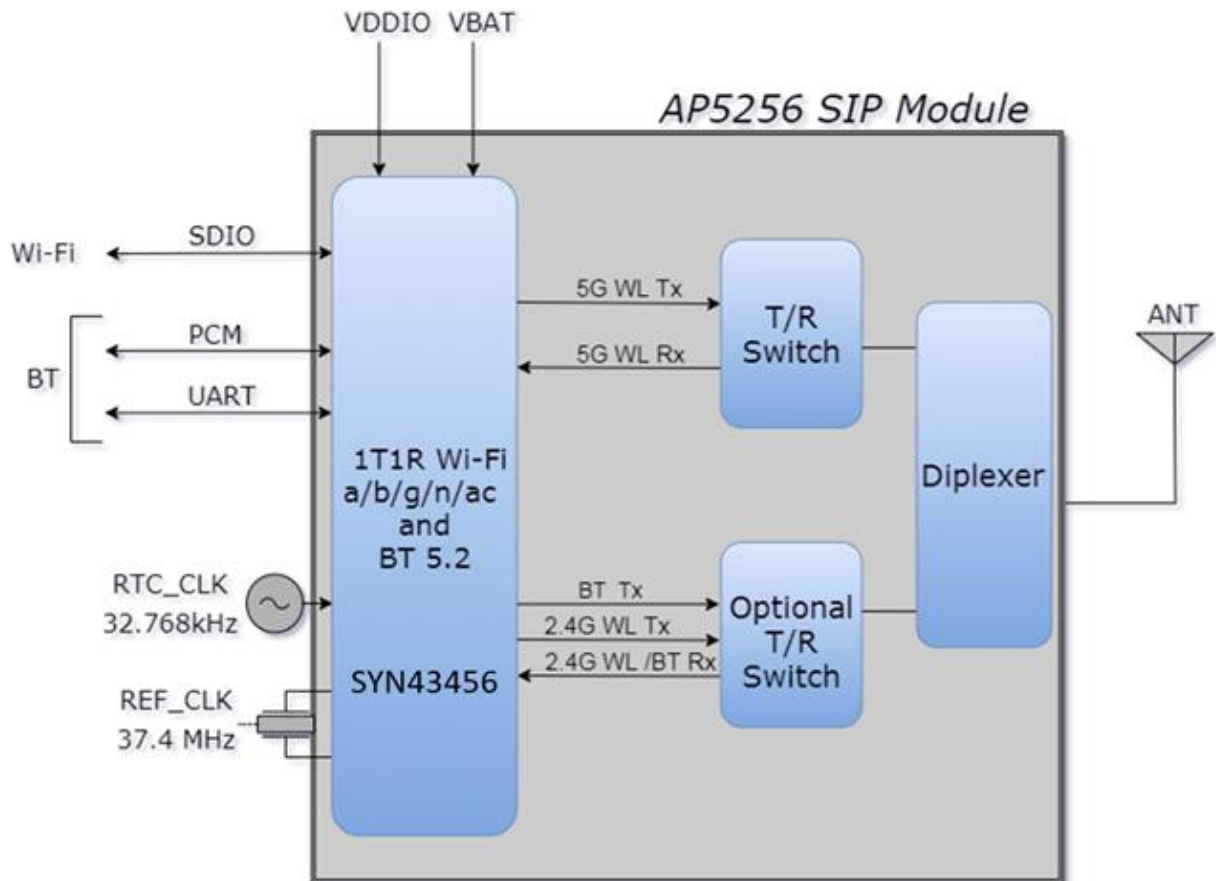


1. Introduction

1.1 Overview

The AMPAK Technology® AP5256 is a fully Wi-Fi and Bluetooth functionalities module with seamless roaming capabilities and advance security, also it could interact with different vendors' 802.11a/b/g/n/ac 1x1 Access Points with SISO standard and can accomplish up to speed of 433.3Mbps with single stream in 802.11ac to connect the wireless LAN. Furthermore AP5256 included SDIO interface for Wi-Fi, UART/ PCM interface for Bluetooth.

In addition, this compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for tablet, OTT box and portable devices.



1.2 Product Features

- Lead free design which is compliant with ROHS requirements.
 - TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
 - Single-stream spatial multiplexing up to 433.3 Mbps data rate.
 - 20, 40, 80 MHz channels with optional SGI (256 QAM modulation)
 - Supports 1antenna with one for WLAN & Bluetooth shared port. Also, shared Bluetooth and WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN.
 - Supports standard SDIO v3.0, compatible with SDIO v2.0 HOST interfaces.
 - BT host digital interface:
 - HCI UART (up to 4 Mbps)
 - PCM for audio data
 - Complies with Bluetooth Core Specification Version 5.2 with provisions for supporting future specifications. With Bluetooth Class 1 or Class2 transmitter operation.
 - Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
 - Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- A simplified block diagram of the module is depicted in the figure above.

2. General Specification

2.1 General Specification

Model Name	AP5256
Product Description	1T1R 802.11 a/b/g/n/ac Wi-Fi + BT 5.2 Module
Dimension	L x W: 8 x 8(Typ.)mm 、 H : 1.5 (Max.) mm
Wi-Fi Interface	SDIO V3.0 / 2.0
BT Interface	UART / PCM
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 125°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -20 °C to +75 °C and 3.2V < VBAT < 3.8V without derating performance.

2.2 DC Characteristics

2.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	4.8	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	3.9	V

2.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
VBAT	3.0	3.3	4.4	V
VDDIO	1.62	1.8 / 3.3	3.63	V

VBAT current consumption 1000mA (Peak), when VBAT = 3.3V



3. Wi-Fi RF Specification

3.1 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11b/g/n & Wi-Fi compliant			
Frequency Range		2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band)			
Number of Channels		2.4GHz：Ch1 ~ Ch13			
Modulation		802.11b：DQPSK、DBPSK、CCK 802.11 g/n：OFDM / 64-QAM、16-QAM、QPSK、BPSK			
Output Power , tolerance ± 1.5 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11b	1Mbps	2Mbps	5.5Mbps	11Mbps	
	17	17	17	17	
802.11g	6、9Mbps	12、18Mbps	24Mbps	36Mbps	48Mbps
	16	16	16	16	15
	54Mbps				
	15				
802.11n 20MHz	MCS0~2	MCS3	MCS4	MCS5	MCS6
	17	17	16	15	14
	MCS7				
	14				
Note：The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.					
Sensitivity, tolerance ± 2 dB					
CCK modulation PER ≤ 8%、OFDM modulation PER ≤ 10%					
802.11b	Data Rate	Spec.(dBm)			
	1Mbps	-96			
	2Mbps	-90			
	5.5Mbps	-88			
	11Mbps	-87			
802.11g	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)	
	6Mbps	-91	24Mbps	-83	
	9Mbps	-88	36Mbps	-80	
	12Mbps	-87	48Mbps	-76	

	18Mbps	-85	54Mbps	-73
802.11n_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS4	-77
	MCS1	-85	MCS4	-75
	MCS2	-84	MCS6	-72
	MCS3	-80	MCS7	-71
Maximum Input Level	802.11b : -10 dBm			
	802.11g/n : -20 dBm			

3.2 5GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11a/n/ac & Wi-Fi compliant			
Frequency Range		5.15~5.35GHz 、 5.47~5.725GHz 、 5.725~5.85GHz （5GHz UNII Band）			
Number of Channels		5.18~5.3GHz ： Ch36 ~ Ch64 5.5~5.72GHz ： Ch100 ~ Ch144 5.745~5.825GHz ： Ch149 ~ Ch165			
Modulation		802.11a ： OFDM / 64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11n ： OFDM / 64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11ac ： OFDM / 256-QAM 、 OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK			
Output Power , tolerance ± 2 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11a	Frequency (MHz)	6~9Mbps	12~18Mbps	24Mbps	36Mbps
	5180~5300	17	17	17	16
	5500~5720	17	17	17	16
	5745~5825	17	17	17	16
	Frequency (MHz)	48Mbps	54Mbps		
	5180~5300	16	15		
	5500~5720	16	15		
	5745~5825	16	15		
802.11n 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5180~5300	17	17	16	15
	5500~5720	17	17	16	15
	5745~5825	17	17	16	15
	Frequency (MHz)	MCS6	MCS7		
	5180~5300	15	14		
	5500~5720	15	14		
	5745~5825	15	14		
802.11n 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5180~5300	17	17	16	16
	5500~5720	17	17	16	16
	5745~5825	17	17	16	16
	Frequency (MHz)	MCS6	MCS7		

	5180~5300	15	14		
	5500~5720	15	14		
	5745~5825	15	14		
802.11ac 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5180~5300	17	17	16	16
	5500~5720	17	17	16	16
	5745~5825	17	17	16	16
	Frequency (MHz)	MCS6	MCS7	MCS8	
	5180~5300	15	14	12	
	5500~5720	15	14	12	
	5745~5825	15	14	12	
802.11ac 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5180~5300	17	17	16	16
	5500~5720	17	17	16	16
	5745~5825	17	17	16	16
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5180~5300	15	14	12	10.5
	5500~5720	15	14	12	10.5
	5745~5825	15	14	12	10.5
802.11ac 80MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5180~5300	17	17	16	16
	5500~5720	17	17	16	16
	5745~5825	17	17	16	16
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5180~5300	15	14	12	10.5
	5500~5720	15	14	12	10.5
	5745~5825	15	14	12	10.5
Note : The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.					
Sensitivity, tolerance ± 2 dB					
CCK modulation PER $\leq 8\%$ 、OFDM modulation PER $\leq 10\%$					
802.11a	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)	
	6Mbps	-92	24Mbps	-82	
	9Mbps	-89	36Mbps	-79	
	12Mbps	-88	48Mbps	-75	
	18Mbps	-86	54Mbps	-74	

802.11n_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-91	MCS4	-78
	MCS1	-88	MCS5	-74
	MCS2	-85	MCS6	-73
	MCS3	-82	MCS7	-71
802.11n_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-89	MCS4	-76
	MCS1	-85	MCS5	-71
	MCS2	-83	MCS6	-70
	MCS3	-79	MCS7	-68
802.11ac_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS5	-73
	MCS1	-87	MCS6	-71
	MCS2	-84	MCS7	-70
	MCS3	-81	MCS8	-67
	MCS4	-77		
802.11ac_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS5	-70
	MCS1	-83	MCS6	-68
	MCS2	-81	MCS7	-66
	MCS3	-78	MCS8	-65
	MCS4	-75	MCS9	-63
802.11ac_80MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-85	MCS5	-69
	MCS1	-82	MCS6	-65
	MCS2	-78	MCS7	-63
	MCS3	-74	MCS8	-61
	MCS4	-71	MCS9	-60
Maximum Input Level	802.11a/n : -20 dBm			
	802.11ac : -30 dBm			

4. Bluetooth Specification

4.1 Bluetooth Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature	Description	
General Specification		
Bluetooth Standard	BDR(1Mbps) 、 EDR(2 、 3Mbps) 、 LE(1 、 2Mbps)	
Host Interface	UART	
Frequency Band	2402 MHz ~ 2480 MHz	
Number of Channels	79 channels for classic 、 40 channels for LE	
Modulation	GFSK, $\pi/4$ -DQPSK, 8DPSK	
RF Specification		
	CL1 (dBm)	CL2 (dBm)
BDR Output Power	6	2
EDR Output Power	4	2
BLE Output Power	5	2
	Typical.	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-88 dBm	
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)	-88 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-85 dBm	
Sensitivity @ PER=30.8% for LE (1Mbps)	-90 dBm	
Sensitivity @ PER=30.8% for LE (2Mbps)	-88 dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm	
	$\pi/4$ -DQPSK (2Mbps) :-20dBm	
	8DPSK (3Mbps) :-20dBm	

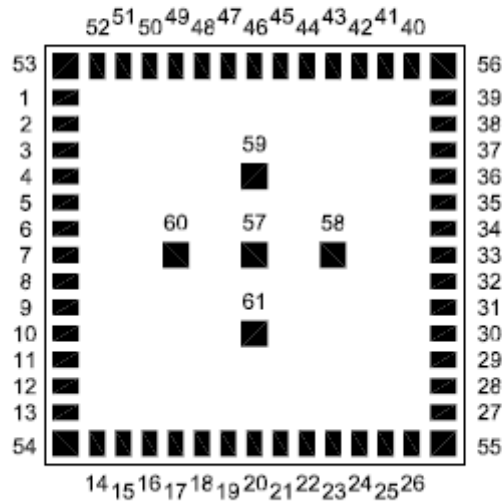
Note* : The Bluetooth output power is able to be configured by firmware (hcd file).



5. Pin Definition

5.1 Pin Outline

<TOP VIEW>



5.2 Pin Assignment

NO	Name	Type	Description
1	GND	—	Ground connections
2	GND	—	Ground connections
3	GND	—	Ground connections
4	GND	—	Ground connections
5	GND	—	Ground connections
6	GND	—	Ground connections
7	GND	—	Ground connections
8	XTAL_IN	I	Crystal input



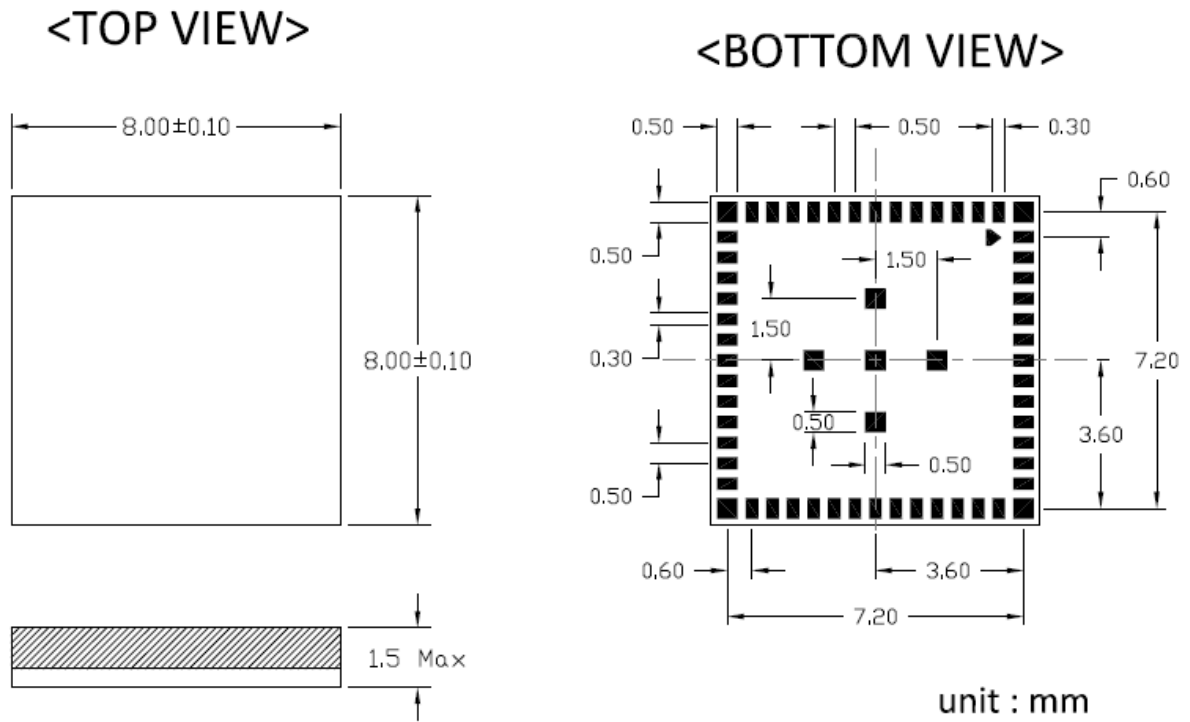
9	XTAL_OUT	O	Crystal output
10	GND	—	Ground connections
11	SDIO_DATA_CMD	I/O	SDIO command line
12	SDIO_DATA_0	I/O	SDIO data line 0
13	SDIO_DATA_1	I/O	SDIO data line 1
14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_CLK	I/O	SDIO clock line
16	SDIO_DATA_3	I/O	SDIO data line 3
17	GND	—	Ground connections
18	VOUT_3P3_IN		Internal LDO 3.3V input.
19	NC	—	Floating (Don't connected to ground)
20	VOUT_3P3		Internal LDO 3.3V output.
21	GND	—	Ground connections
22	VBAT	P	Main power voltage source input
23	GND	—	Ground connections
24	VIO	P	I/O Voltage supply input
25	GND	—	Ground connections
26	VDD_CBUCK_1P5	P	Internal CBUCK voltage input generation pin
27	SR_VLX	P	Internal CBUCK switching regulator output generation pin
28	GND	—	Ground connections
29	SDIO_VSEL	I	SDIO mode selection pin 1 : 1.8V(SDIO 2.0/3.0), 0 : 3.3V(SDIO 2.0 only) WL_GPIO_7
30	GND	—	Ground connections
31	LPO_IN	I	External Low Power Clock input (32.768KHz)
32	GND	—	Ground connections
33	BT_PCM_SYNC	I/O	PCM sync signal
34	BT_PCM_IN	I	PCM data input
35	BT_PCM_CLK	I/O	PCM clock
36	BT_PCM_OUT	O	PCM Data output
37	NC	—	Floating (Don't connected to ground)
38	BT_UART_RTS_N	O	Bluetooth UART interface
39	BT_UART_TXD	O	Bluetooth UART interface
40	BT_UART_RXD	I	Bluetooth UART interface
41	BT_UART_CTS_N	I	Bluetooth UART interface



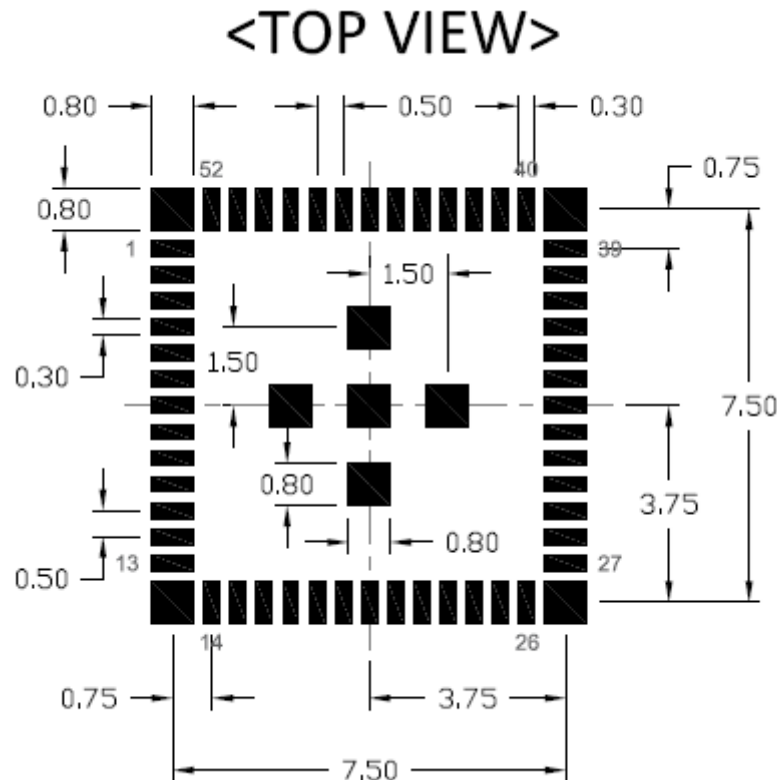
42	GND	—	Ground connections
43	WL_HOST_WAKE	O	WLAN to wake-up HOST
44	WL_REG_ON	I	Power up/down internal regulators used by Wi-Fi section
45	WL_GPIO_6	I/O	WL_GPIO_6 configuration pin
46	BT_WAKE	I	HOST wake-up Bluetooth device
47	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
48	BT_CLK_REQ		Reference clock request
49	BT_REG_ON	I	Power up/down internal regulators used by BT section
50	GND	—	Ground connections
51	RF_PORT	I/O	RF I/O port
52	GND	—	Ground connections
53	GND	—	Ground connections
54	GND	—	Ground connections
55	GND	—	Ground connections
56	GND	—	Ground connections
57	GND	—	Ground connections
58	GND	—	Ground connections
59	GND	—	Ground connections
60	GND	—	Ground connections
61	GND	—	Ground connections

6. Dimensions

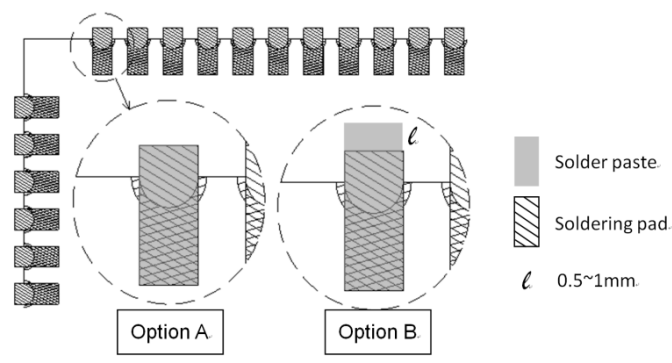
6.1 Module Dimensions



6.2 Recommended footprint



- Solder paste layer design is generally the same as recommended footprint.
(錫膏層設計通常建議和焊墊尺寸相同)
- If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial.
In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact AMPAK FAE for assistance.
(如果模組吃錫品質考量側面爬錫，如何優化鋼網開孔設計以調整適當的錫膏量是非常重要的。尤其鋼網的厚度大約是 0.1mm 或更薄時，可考慮局部加厚鋼網的設計。請諮詢製程工程師以優化鋼網的設計,或是聯絡正基科技技術支持團隊)。



7. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-25	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 3300	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	>100k	Ω
	<5	pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7V _{io} - V _{io}	V

External 37.4MHz X'TAL characteristics

Parameter	Specification	Units
Nominal frequency - F ₀	37.4	MHz
Frequency Tolerance - $\Delta F / F_0$ (At 25°C +/- 3°C)	+/- 10	ppm
Operation Temperature Range - Topr	-30 ~ + 85	°C
Freq. Stability(over operating temperature) - TC Ref. to 25°C	+/- 10	ppm
Load capacitance - CL	18	pF
Equivalent Series Resistance – ESR	Max. 60	Ω
Drive Level - DL	Typ. 50, Max. 100	μ W
Insulation resistance – IR At 100Vdc	Min. 500	M Ω



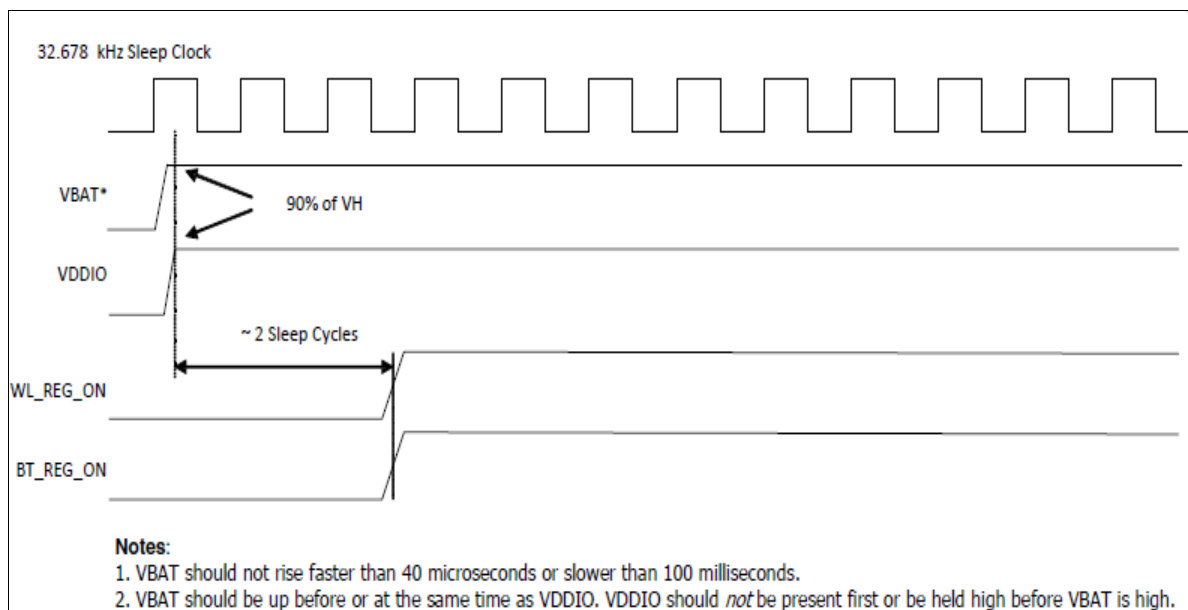
8. Host Interface Timing Diagram

8.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

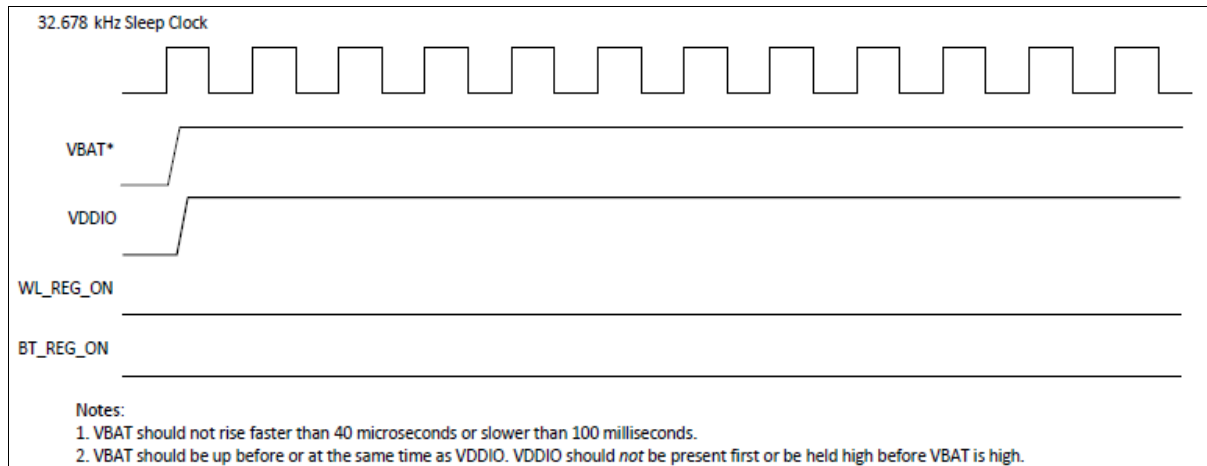
Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

- **WL_REG_ON**: Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- **BT_REG_ON**: Used by the PMU to power up or power down the internal regulators used by the BT section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).

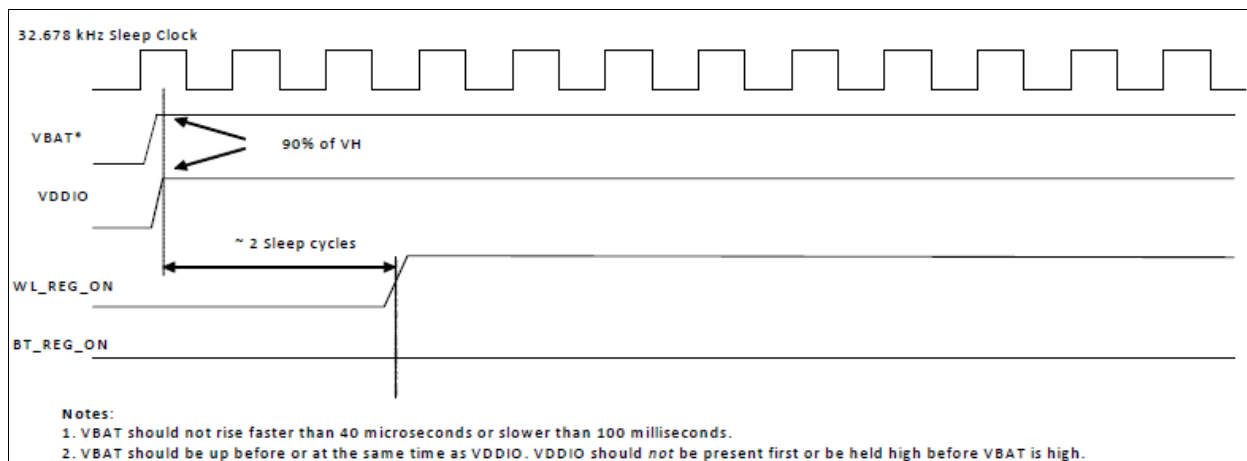


WLAN=ON, Bluetooth=ON

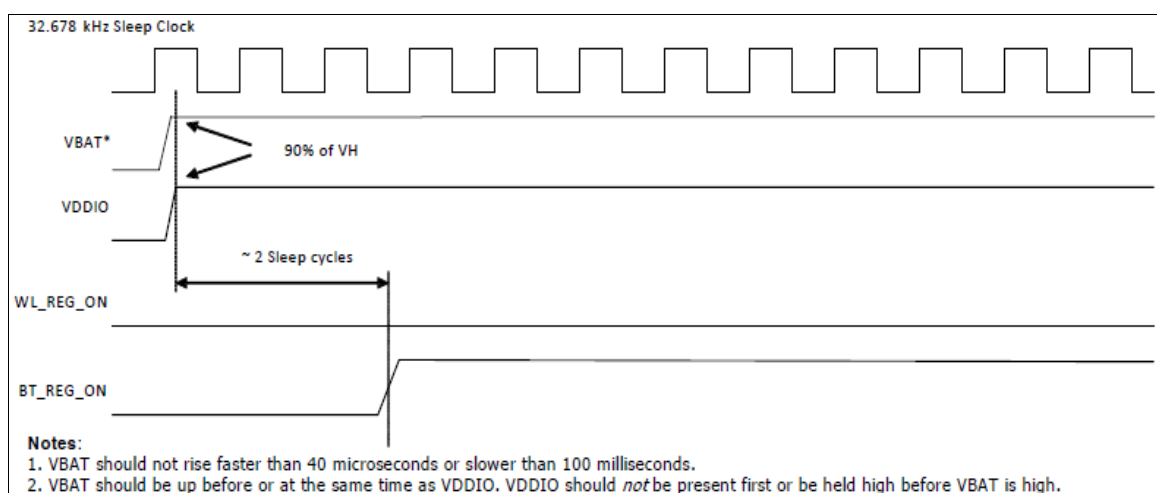




WLAN=OFF, Bluetooth=OFF



WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON



8.2 SDIO Interface Description

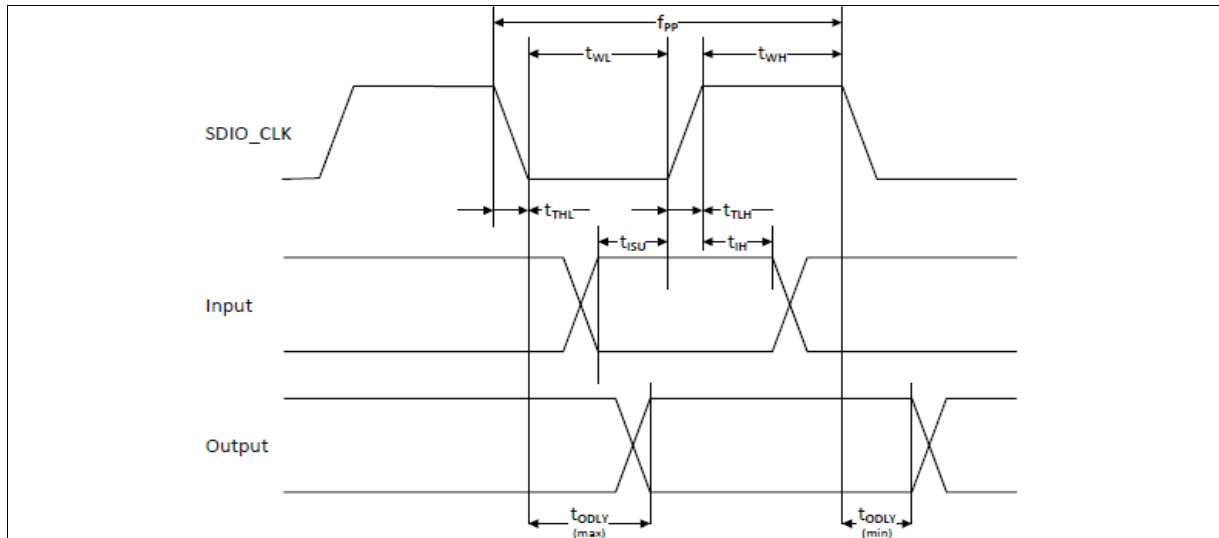
The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50(100Mbps), DR104(208MHz) and DDR50(50MHz, dual rates) in addition to the 3.3V default speed(25MHz) and high speed (50 MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- Function 0 Standard SDIO function (Max Block Size / Byte Count = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max Block Size / Byte Count = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max Block Size/Byte Count=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

SDIO Default Mode Timing Diagram

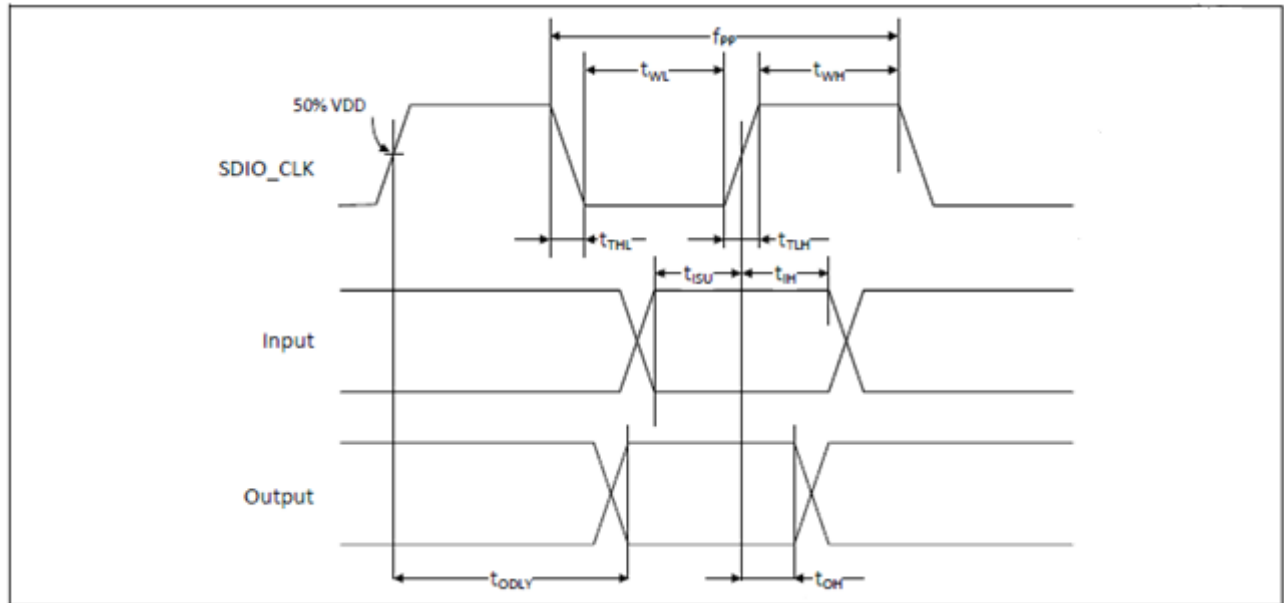


Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL^b)					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

- a. Timing is based on $CL \leq 40pF$ load on CMD and Data.
 b. $\min(V_{ih}) = 0.7 \times V_{DDIO}$ and $\max(V_{il}) = 0.2 \times V_{DDIO}$.

SDIO High Speed Mode Timing Diagram





Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency – Data Transfer Mode	f _{PP}	0	–	50	MHz
Frequency – Identification Mode	f _{OD}	0	–	400	kHz
Clock low time	t _{WL}	7	–	–	ns
Clock high time	t _{WH}	7	–	–	ns
Clock rise time	t _{TLH}	–	–	3	ns
Clock low time	t _{THL}	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	t _{ISU}	6	–	–	ns
Input hold Time	t _{IH}	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	t _{ODLY}	–	–	14	ns
Output hold time	t _{OH}	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

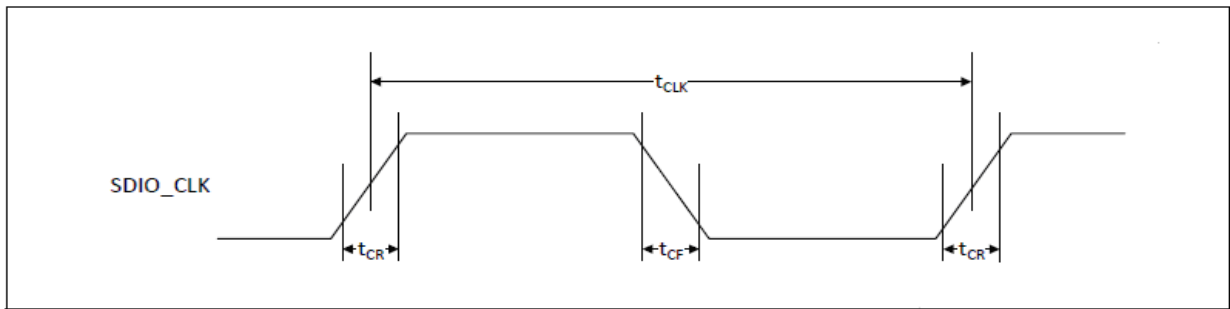
a. Timing is based on $CL \leq 40$ pF load on CMD and Data.

b. $\min(V_{IH}) = 0.7 \times V_{DDIO}$ and $\max(V_{IL}) = 0.2 \times V_{DDIO}$.

SDIO Bus Timing Specifications in SDR Modes

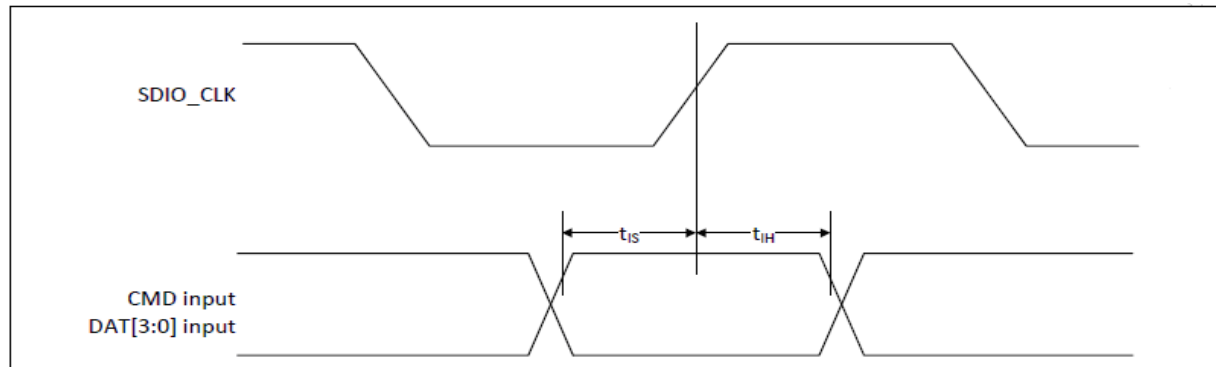


Clock Timing (SDR Modes)



Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		10	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00$ ns (max) @100 MHz, $C_{CARD} = 10$ pF $t_{CR}, t_{CF} < 0.96$ ns (max) @208 MHz, $C_{CARD} = 10$ pF
Clock duty	–	30	70	%	–

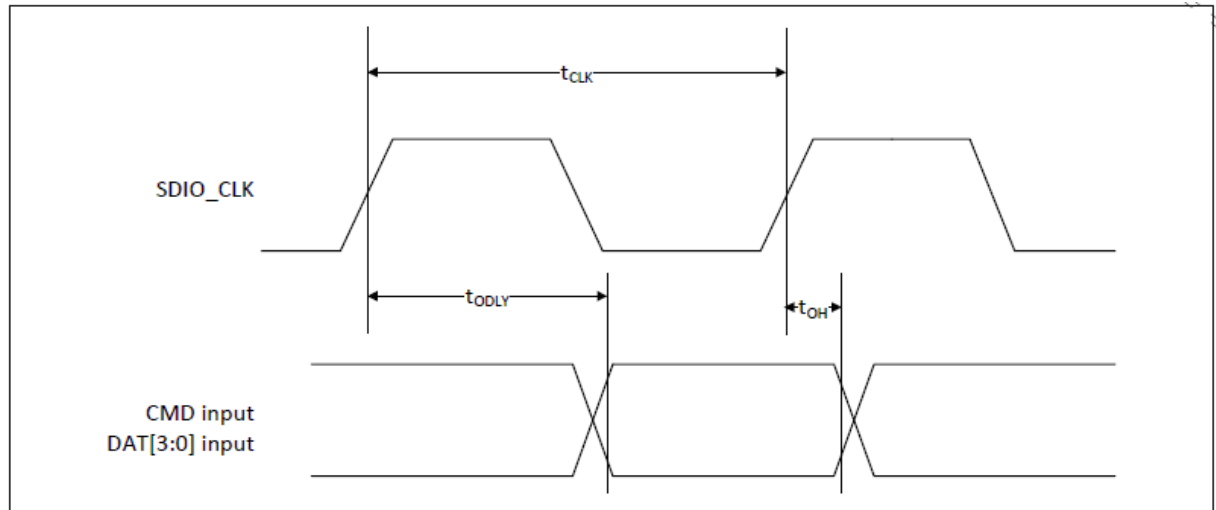
SDIO Bus Input Timing (SDR Modes)



Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	–	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	–	ns	$C_{CARD} = 5$ pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	–	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	–	ns	$C_{CARD} = 5$ pF, VCT = 0.975V

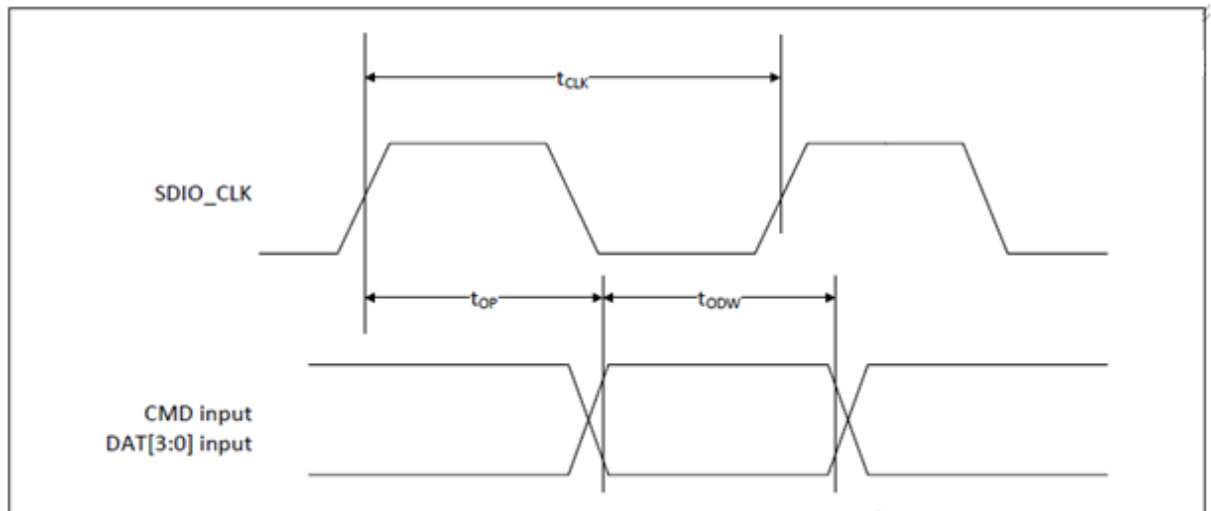
SDIO Bus Output Timing (SDR Modes up to 100MHz)





Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	$t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) $C_L = 15$ pF

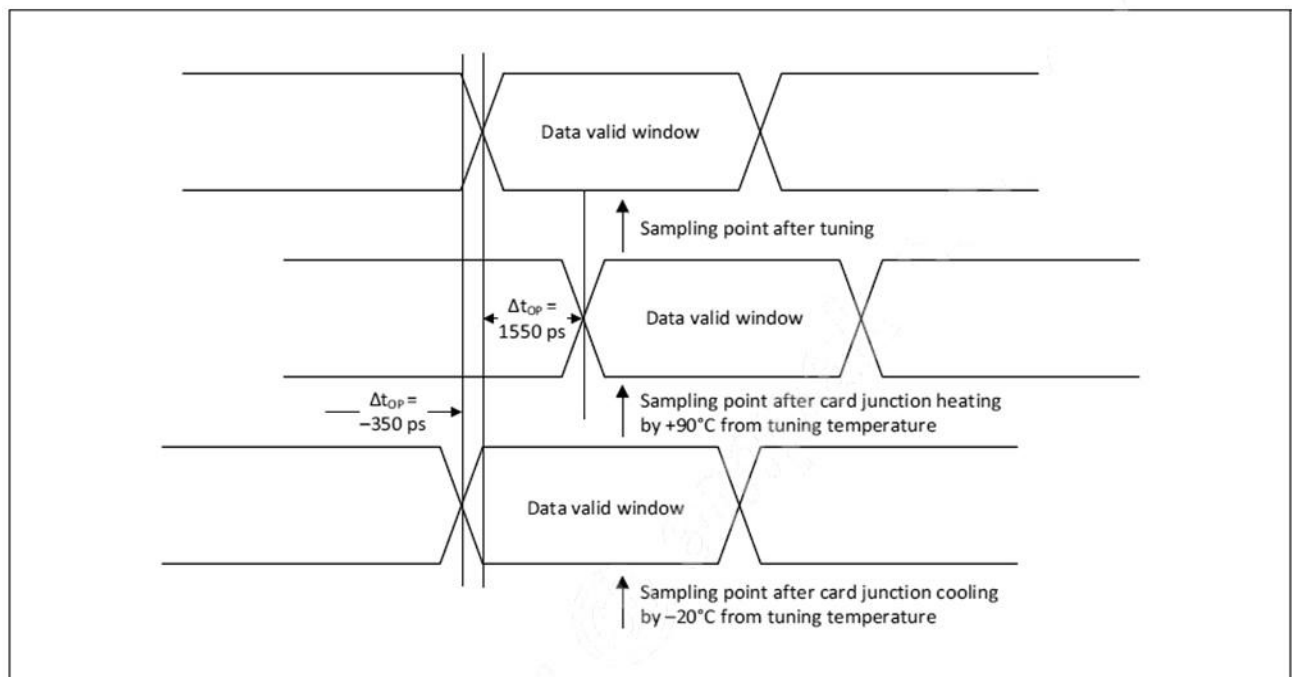
Card Output Timing (SDR Modes 100MHz to 208MHz)



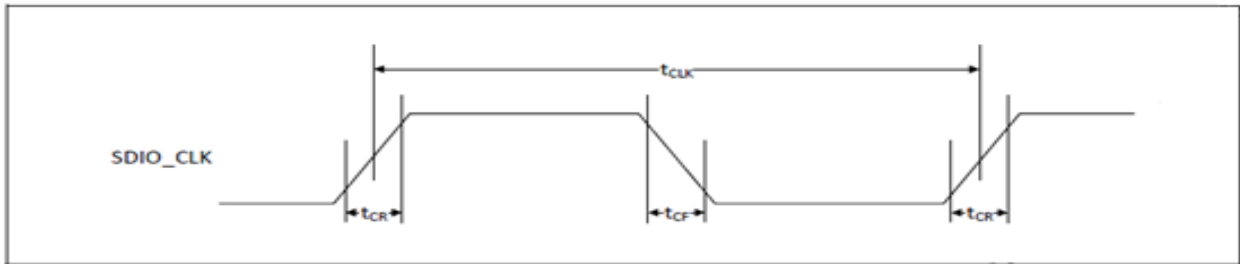
Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	$t_{ODW}=2.88$ ns @208 MHz

- $\Delta t_{OP} = +1550$ ps for junction temperature of $\Delta t_{OP} = 90$ degrees during operation
- $\Delta t_{OP} = -350$ ps for junction temperature of $\Delta t_{OP} = -20$ degrees during operation
- $\Delta t_{OP} = +2600$ ps for junction temperature of $\Delta t_{OP} = -20$ to $+125$ degrees during operation

Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)

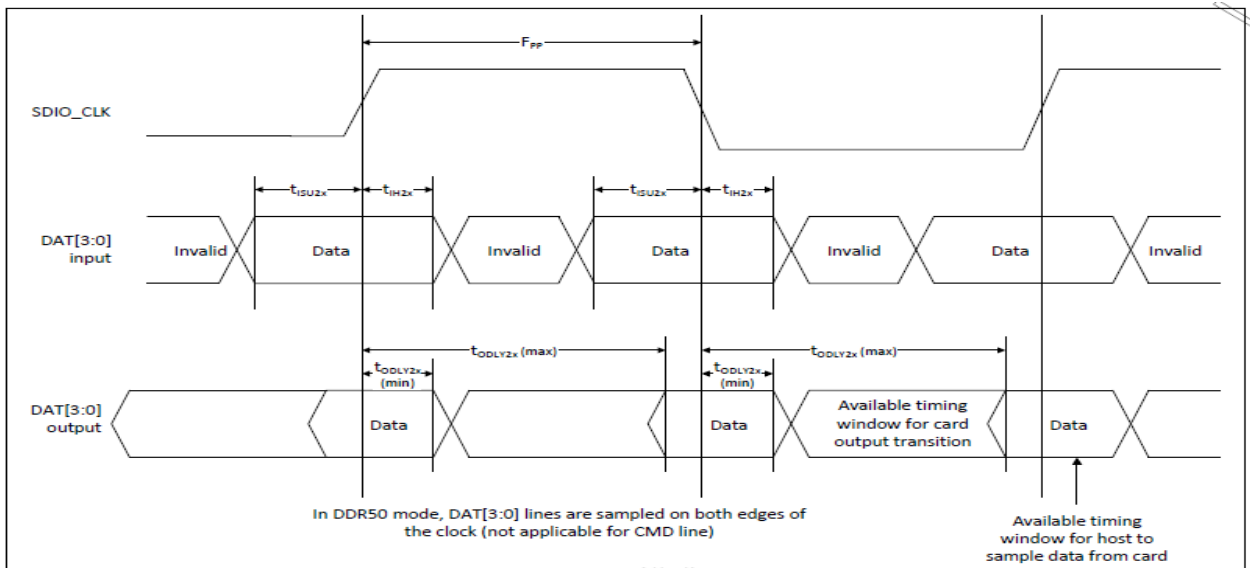


SDIO Bus Timing Specifications in DDR50 Mode



Parameter	Symbol	Minimum	Maximum	Unit	Comments
—	t_{CLK}	20	—	ns	DDR50 mode
—	t_{CR}, t_{CF}	—	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00$ ns (max) @50 MHz, $C_{CARD} = 10$ pF
Clock duty	—	45	55	%	—

Data Timing



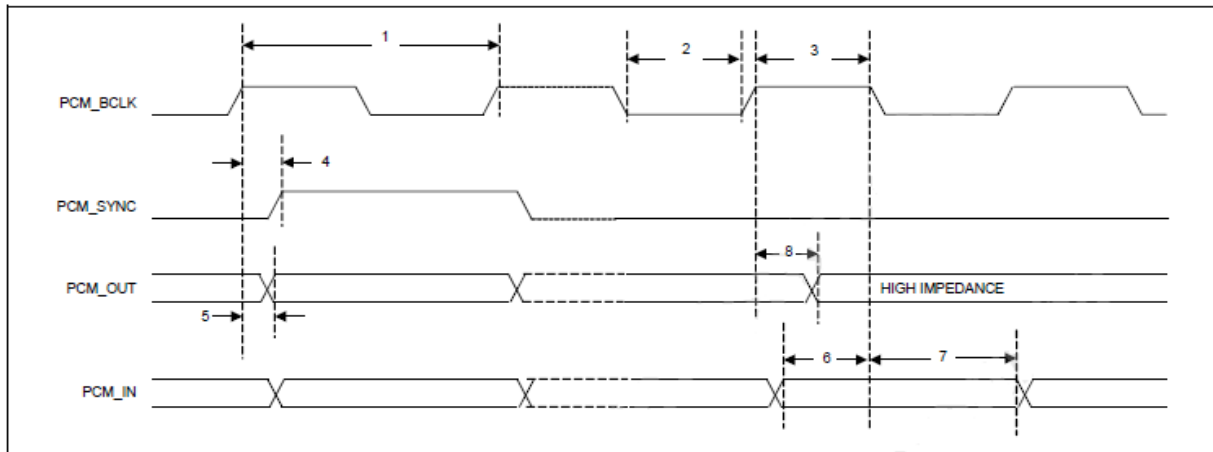
Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	—	ns	$C_{CARD} < 10$ pF (1 Card)
Input hold time	t_{IH}	0.8	—	ns	$C_{CARD} < 10$ pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	—	13.7	ns	$C_{CARD} < 30$ pF (1 Card)
Output hold time	t_{OH}	1.5	—	ns	$C_{CARD} < 15$ pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	—	ns	$C_{CARD} < 10$ pF (1 Card)
Input hold time	t_{IH2x}	0.8	—	ns	$C_{CARD} < 10$ pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	—	7.5	ns	$C_{CARD} < 25$ pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	—	ns	$C_{CARD} < 15$ pF (1 Card)

8.3 PCM Interface Description

The PCM Interface on the BCM43456 can connect to linear PCM Codec devices in master or slave mode. In master mode, the BCM43456 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the BCM43456. The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Short Frame Sync, Master Modem

PCM Timing Diagram (Short Frame Sync, Master Mode)



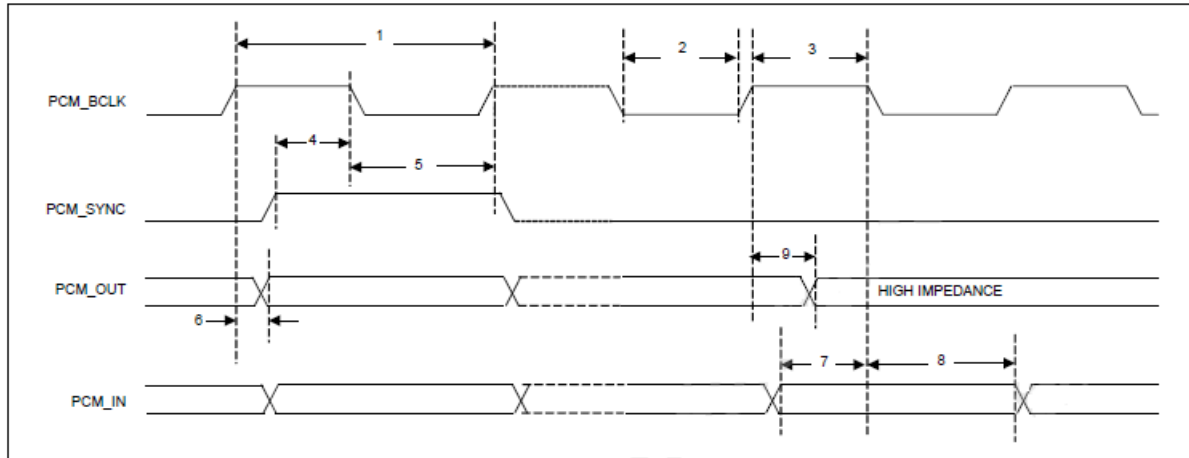
PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns



Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)



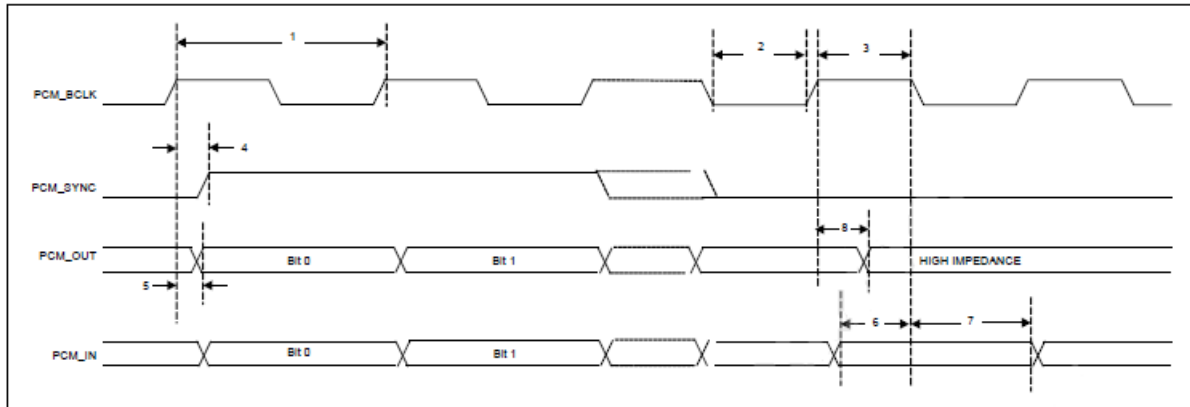
PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns



Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)



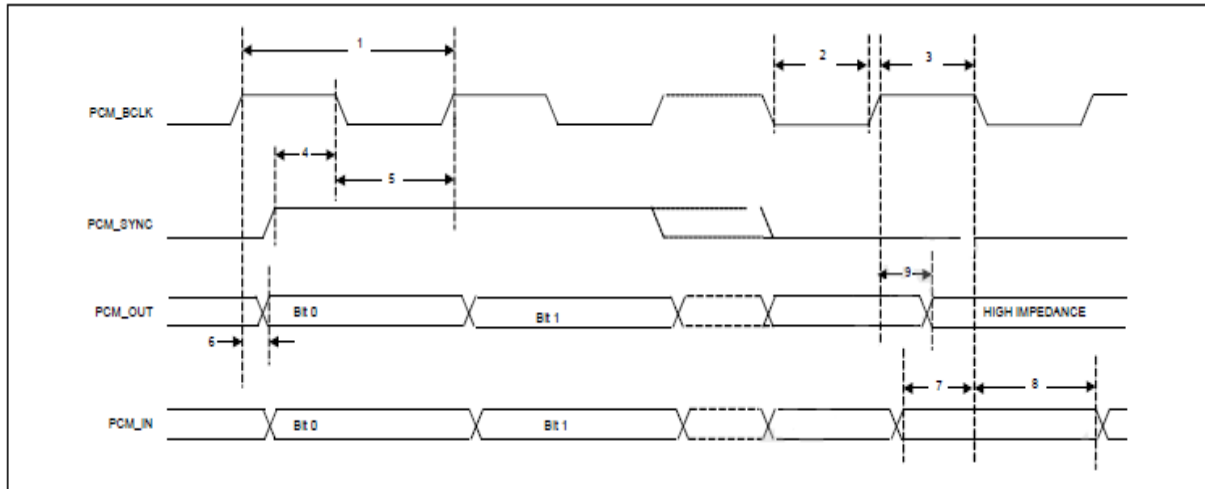
PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns



Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)



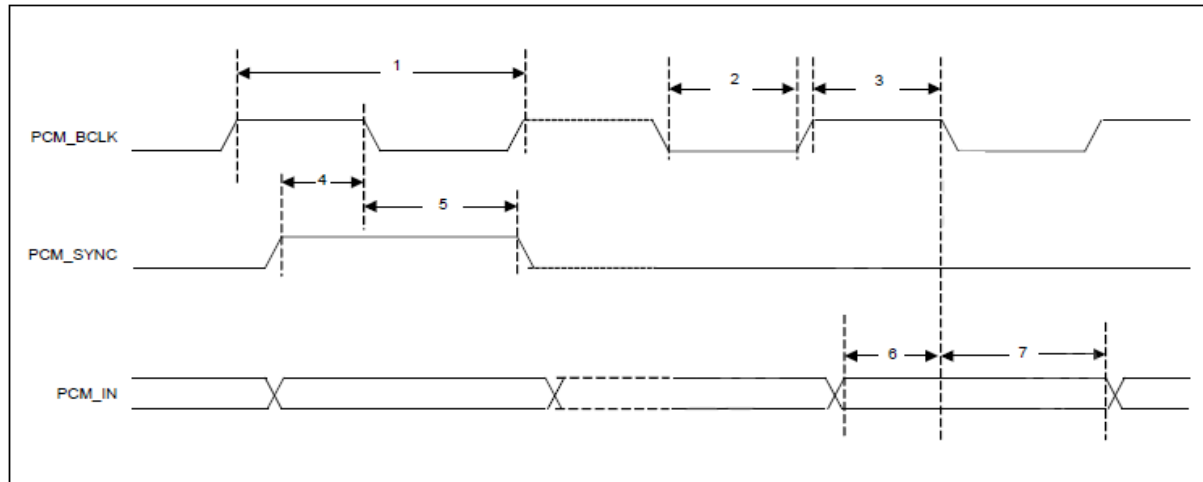
PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns



Short Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Short Frame Sync)



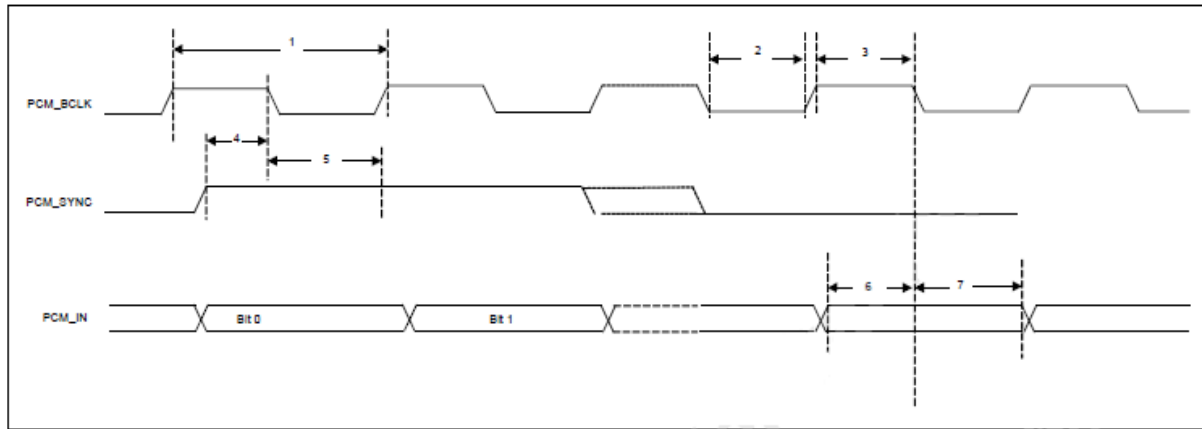
PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns



Long Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Long Frame Sync)



PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns



8.4 UART Interface Description

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The BCM43456 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

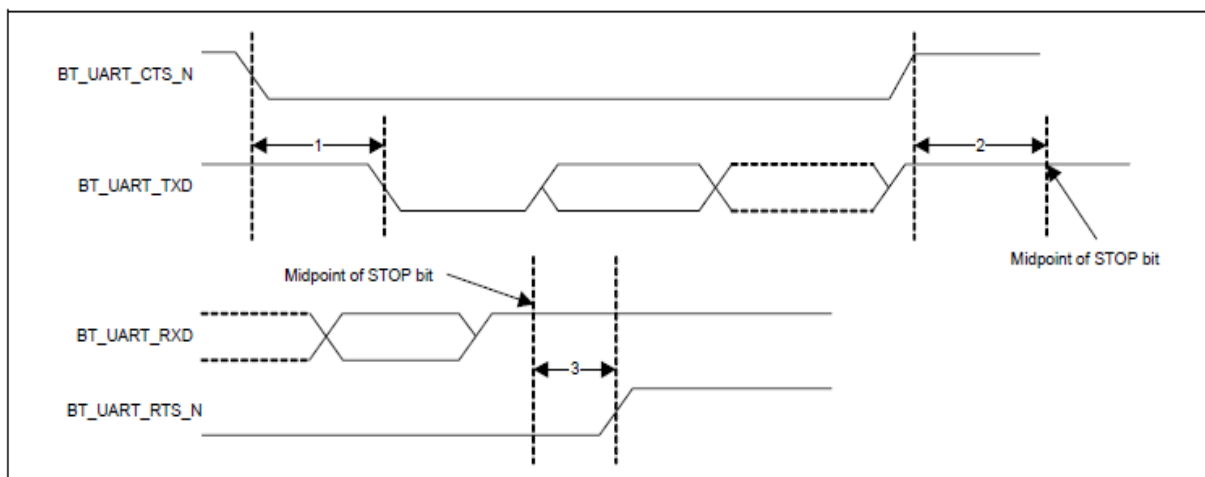
Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The BCM43456 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within $\pm 2\%$.



Example of Common Baud Rates

<i>Desired Rate</i>	<i>Actual Rate</i>	<i>Error (%)</i>
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

UART Timing

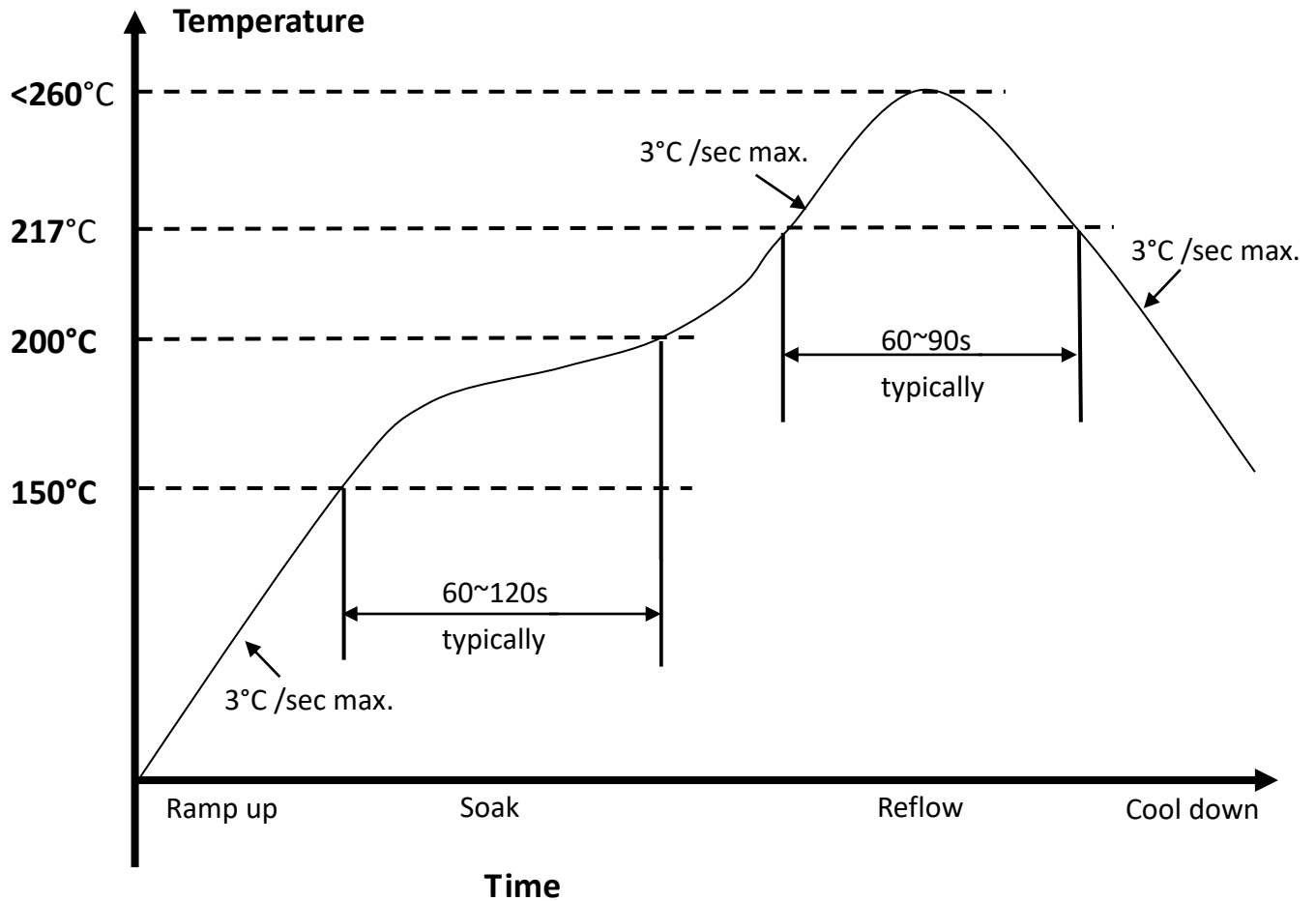


UART Timing Specifications

<i>Ref</i>	<i>Characteristics</i>	<i>Min.</i>	<i>Typ.</i>	<i>Max.</i>	<i>Unit</i>
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods



9. Recommended Reflow Profile



1. Referred to IPC/JEDEC standard
2. Peak Temperature : <260°C
3. Cycle of Reflow: 2 times max.
4. Adding Nitrogen (N₂) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component

10. Package Information

10.1 Label

Label A → Anti-static and humidity notice



Label B → MSL caution / Storage Condition

Caution		LEVEL
This bag contains MOISTURE-SENSITIVE DEVICES		☐
If blank, see adjacent bar code label		
1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)		
2. Peak package body temperature: _____ °C If blank, see adjacent bar code label		
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be		
a) Mounted within: _____ hours of factory conditions If blank, see adjacent bar code label		
b) Stored per J-STD-033		
4. Devices require bake, before mounting, if:		
a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C		
b) 3a or 3b are not met		
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure		
Bag Seal Date: _____ If blank, see adjacent bar code label		
Note: Level and body temperature defined by IPC/JEDEC J-STD-020		

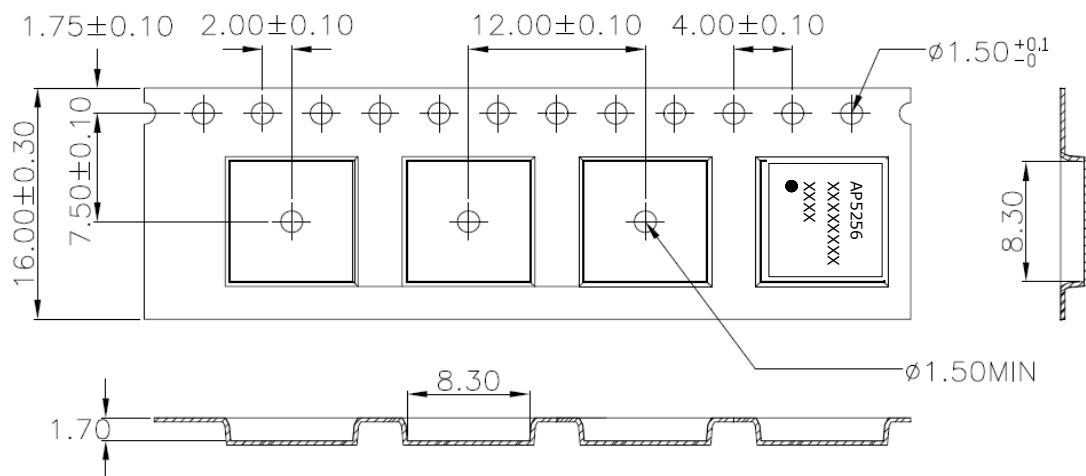
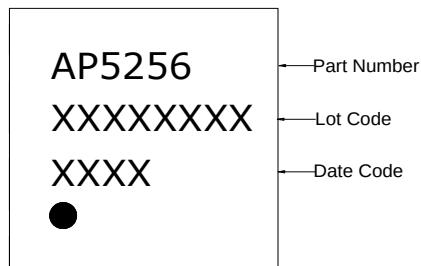
Label C → Inner box label .

PO:	
AMK DEVICE:	
PKG S/N:	
Model Name:	9PKGYYMMDDnnnnn AP5256 (R3HF)
P/N:	
Quantity:	99P-W01-0XXXR
Date Code:	
Lot Code:	YYWW XXXXXXX
	Made in XXXXXX

Label D → Carton box label .

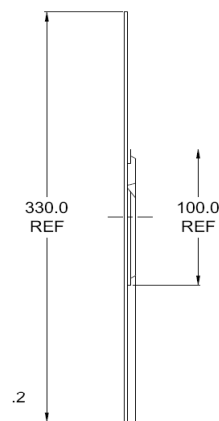
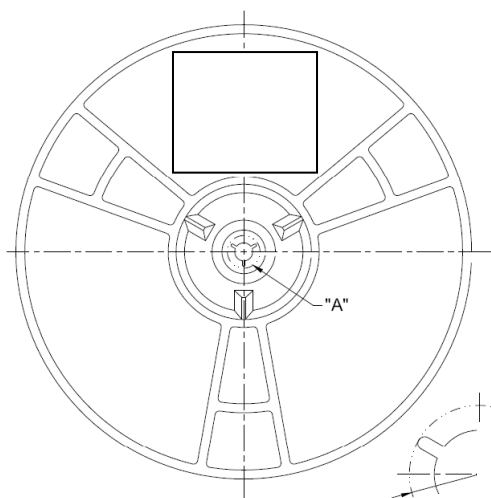
AMPAK Technology Inc.	
PO:	
AMK DEVICE:	
Model Name:	AP5256 (R3HF)
Part No.:	
Quantity:	99P-W01-0XXXR
Lot D/C:	Q000 XXXXXXX YYWW Q000
Manufacture:	
	YYYYMMDD Made in XXXXXX

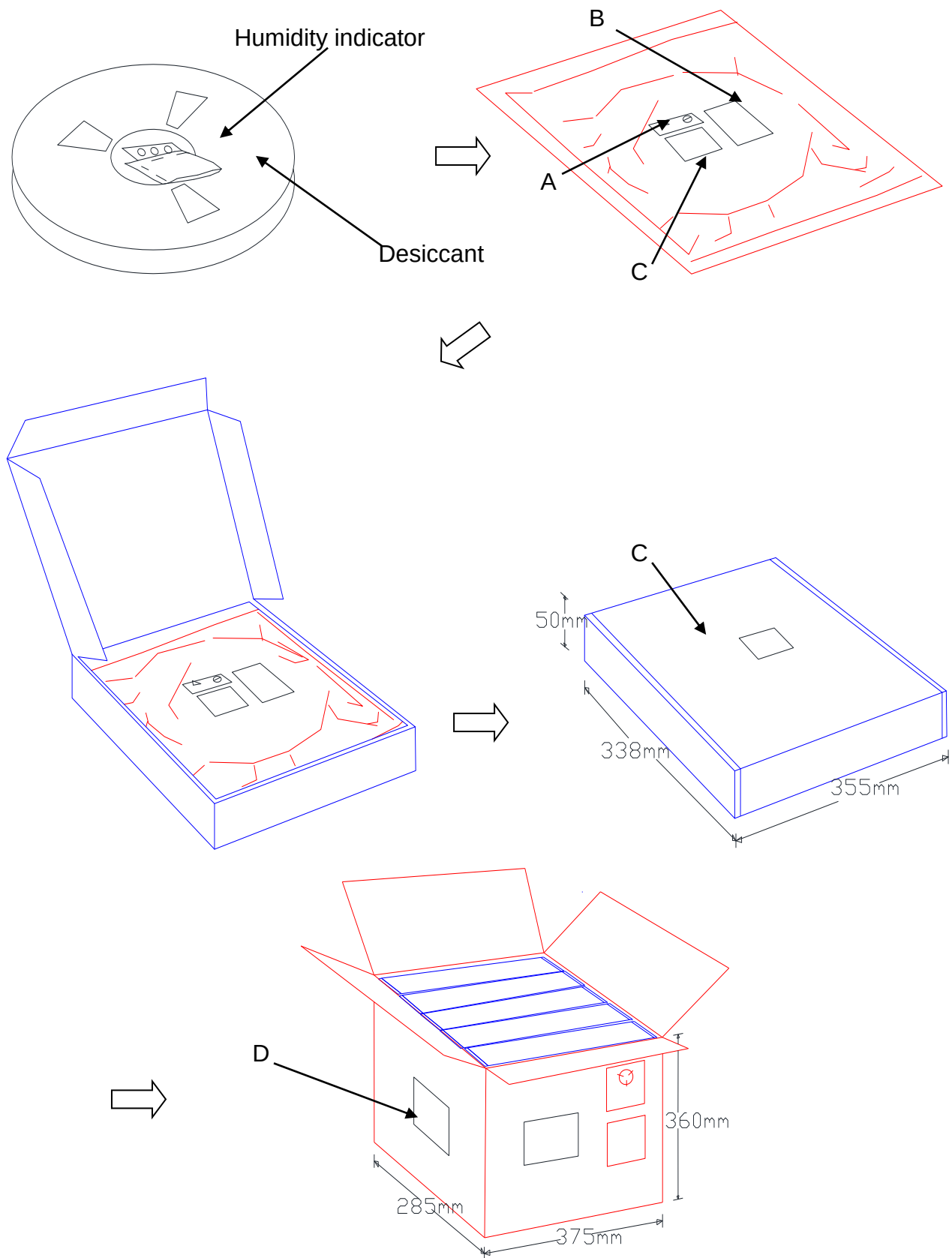
10.2 Packing



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30 ± 0.05 mm.
6. Component load per 13" reel : 1500 pcs

W	16.00±0.30
A0	8.30±0.10
B0	8.30±0.10
K0	1.70±0.10





10.3 MSL Level / Storage Condition

	Caution This bag contains MOISTURE-SENSITIVE DEVICES	LEVEL 4
If blank, see adjacent bar code label		
1. Calculated shelf life in sealed bag: 12 months at $<40^{\circ}\text{C}$ and $<90\%$ relative humidity (RH)		
2. Peak package body temperature: <u>250</u> $^{\circ}\text{C}$ If blank, see adjacent bar code label		
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be		
a) Mounted within: <u>72</u> hours of factory conditions If blank, see adjacent bar code label		
$\leq 30^{\circ}\text{C} / 60\% \text{ RH, or}$		
b) Stored per J-STD-033		
4. Devices require bake, before mounting, if:		
a) Humidity Indicator Card reads $>10\%$ for level 2a-5a devices or $>60\%$ for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$		
b) 3a or 3b are not met.		
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.		
Bag Seal Date: _____ If blank, see adjacent bar code label		
Note: Level and body temperature defined by IPC/JEDEC J-STD-020		